

Time evolution of frequency components in a chaotic digital signal

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ABSTRACT

The type of signals obtained has conditioned chaos analysis tools. Almost in every case, they have analogue characteristics. But in certain cases, a chaotic digital signal is obtained and these signals need a different approach than conventional analogue ones. The main objective of this paper will be to present some possible approaches to the study of these signals and how information about their characteristics may be obtained in the more straightforward possible way.

We have obtained digital chaotic signals from an Optical Logic Cell with some feedback between output and one of the possible control gates. This chaos has been reported in several papers and its characteristics have been employed as a possible method to secure communications and as a way to encryption. In both cases, the influence of some perturbation in the transmission medium gave problems both for the synchronization of chaotic generators at emitter and receiver and for the recovering of information data. A proposed way to analyze the presence of some perturbation is to study the noise contents of transmitted signal and to implement a way to eliminate it. In our present case, the digital signal will be converted to a multilevel one by grouping bits in packets of 8 bits and applying conventional methods of time-frequency analysis to them. The results give information about the change in signals characteristics and hence some information about the noise or perturbations present. Equivalent representations to the phase and to the Feigenbaum diagrams for digital signals are employed in this case.

Keywords: Digital chaos, Route to chaos, Chaos evolution

1. INTRODUCTION

The analyses of chaotic signals have been one of the main topics of research in the last years. This analysis has been always performed by analytical methods almost since the beginning of their study. This was due to the analogue character of the involved signals. But in some cases, the chaotic signal has a digital character and the conventional methods are no longer valid. This is the case for the chaotic signal obtained from Optical Logic Cells when some feedback is applied from one of the possible outputs to one of the control gates. We have studied this situation in several papers. The main problem with this signal is that analytical methods cannot be applied to the resulting chaotic signal. To extract its characteristics is not possible with the methods employed in other analogue cases.

We have proposed several methods in the last years. Every one of them has been based in a new type of phase diagram where binary data were converted to the hexadecimal system. The binary signals are, in this way, converted to a multilevel signal. Signals at a particular time are represented as a function of the signal at the previous time interval. A periodic signal appears, in this representation, as a closed figure and a chaotic one offers a time evolution without any particular recovery of previous positions. This type of analysis is convenient when an indication about the signal characteristics need to be known. The information extracted from it corresponds to the total behaviour of the system and, although each point corresponds to particular time, the represented image is the total time evolution of the system without the possibility to infer the time corresponding to each point. Moreover, there is not any possibility to know the characteristics of the signal at a particular interval.

In some cases is necessary to know how a chaotic state has been obtained and how has been the route to chaos. A chaotic system, for instant, is not chaotic from the very beginning of its initial point. It needs a certain time to stabilize and

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to get the final state where a real chaotic behavior is present. We have analyzed this and it has been shown that after a certain interval of time, normally between 100 and 150 bit time intervals, the situation may be considered close to chaos. If the system parameters are the adequate, chaos may be achieved. This has been studied by the Lempel and Ziv complexity measure and allows handling a numerical method to analyze the particular situation at a particular time. We shall return to this point in a further paragraph.

Moreover, there are some other situations that may need another different type of analysis. They are, for example, when the critical parameter that determines the possibility to obtain chaos is known. As it is very well known from conventional chaos theory, when this parameter changes its value, a sequence of different behaviors appear in the system. If at some initial value the behavior is approaching to a stationary state, some change in the parameter value may conduct the system to an oscillatory condition. Further parameter variations, change the value of the resulting frequencies giving rise to new frequencies that follow a certain pattern: the number of frequencies double, multiply by four, by eight, ... This is known as frequency doubling. Finally, at a determined parameter value, the situation of the system may arrive to a chaotic state. The whole collection of states is known as the "rote to chaos" and when it is represented gets the name of Feigenbaum Diagram.

Feigenbaum diagram represents one of the more direct ways to know the real behavior of any chaotic systems. It indicate the values of the critical parameter where the system adopts a particular behavior and how we have to change its value to achieve a certain situation. This diagram shows those regions where there are periodic situations and irregular behaviors. Because the transition points from a region to another are very precise it is possible to locate the system at a convenient situation for a particular evolution.

The analysis of this type of diagram is very well known for analog signals and for phenomena ruled by algebraic or discrete equations. One of the more popular is the logistic equation. The ways to solve it have been numerous in the last

years, ranging from techniques as Taylor series, Galerkin solutions, and Runge-Kuta. Robert May¹ pointed out that simple mathematical models could represent very complicated mathematics. He studied the evolution of future population as a function of previous generations. He showed that the progress of dynamic systems could be described graphically with the use of quadratic map. In some cases an imaginary iteration machine may represent this progress and the evolution of the system described as the evolution of its states. The iterations, when represented as a function of the changing parameter, offered a clear indication of the system transition in time. The diagram give the possibility to know regions where there are stable points, where periodic situations, where instabilities and, finally, where chaotic situations. From these types of diagrams, certain universal numbers, known as the Feigenbaum universal numbers, are obtained. But as before, most of the cases where this diagram has been obtained have been situations with a large

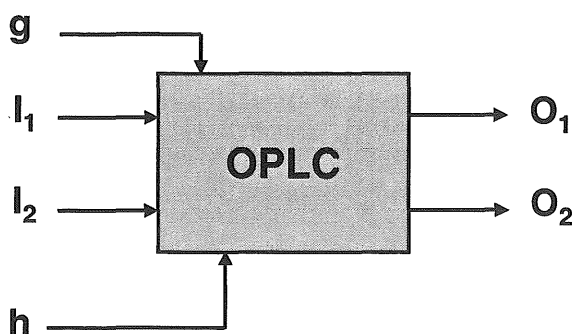


Fig. 1.- General configuration of the Optically Programmable Logic Cell.

variety of resulting number. The analyzed systems were multivalued. In our present case, situation deals just with two possible output states, namely, bits "1" and "0".

The present paper will try to obtain a method to analyze binary systems with nonlinear behaviour and extract some consequences about the possible techniques to know its evolution in time.

2. CHAOTIC SIGNAL TO BE ANALYZED

The signal analyzed in this paper has been obtained from an Optically Programmable Logic Cell employed as basic unit to construct arithmetical units. Although the basic unit to be employed here has been reported previously in several papers²⁻³, some details will be presented here. They will be employed in our present work. Its basic configuration appears in Fig. 1. Input and output signals are optical binary data and the employed devices, non-linear optoelectronic devices with digital characteristics. Fig. 1 shows a block representation of the basic cell. Two optical devices, P and Q, with a non-linear

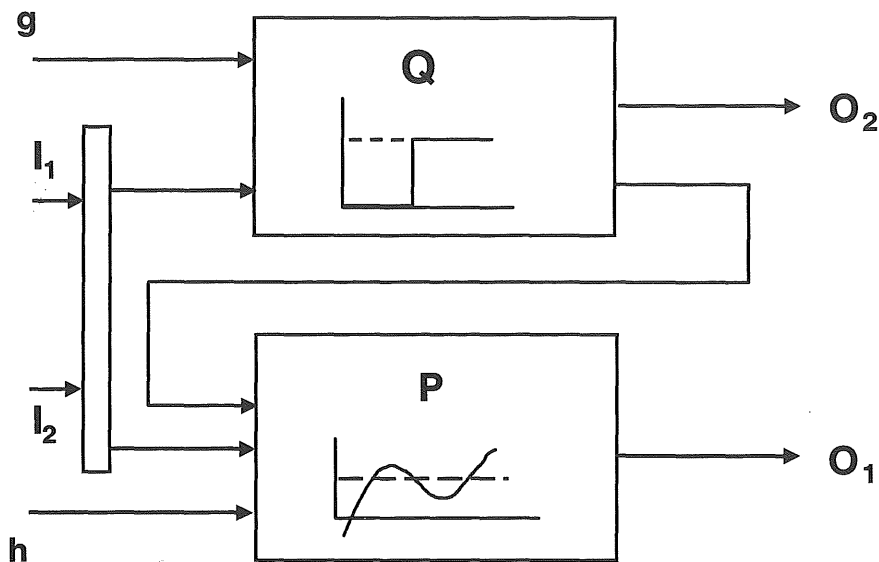


Fig. 2.- Internal configuration of the OPLC.

behaviour, compose the circuit. The outputs of each one of them correspond to the two final outputs, O_1 and O_2 , of the cell. The possible inputs to the circuit are four. Two of them are for input data, I_1 e I_2 , and the other two, g and h , for control signals. The corresponding inputs to the non-linear devices, P and Q , are functions of these signals plus, in the case of the P device, one other coming from inside the own cell and obtained from the Q device. Some details about the internal connections of the cell are shown in Fig. 2. More details may be seen in other papers^{4,11}.

This structure has several properties that deserve some details. When it works in a "linear" regime it is able to operate as a logic cell. It offers, at the output, up to fifteen pairs of logic functions of the two binary inputs. It is this functioning the one that allows us to employ it as basic unit to construct circuits as half full-adders and full-adders. This structure has been computer simulated and works in the laboratory with an optoelectronic configuration and optical fibers as connecting elements.

When a feedback is applied between one of the outputs and a control gate, a nonlinear regime start to appear. This nonlinear regime depends on two main parameters. These parameters are related to the times needed to be the signal feed backed and the needed by the circuit to process the signal. The first one will be called "external time" and the second on "internal time". The absolute value of these two times is no really important. The parameter that is really important is the relation between them. The relation to be studied is the ratio between the external time and the internal. This quotient is, in some way, similar to the critical parameter employed in the logistic equation. Its variations affects to the behaviour of the system.

The way to study the signals obtained from a circuit as the above described is not an easy task. The main difficulty comes from the fact that the signal has a binary character. It is composed just by "1"s and "0"s. Under these circumstances it is impossible to represent common diagrams as the phase diagram because if one should try to do it, it should get just a square with four points. Hence, no information should be obtained. We have solved this problem by converting the initial bits pattern in a sequence of new digits obtained from the initial ones. These new digits are the corresponding hexadecimal values of the bits arranged in groups of four bits. In this way, the number of bits have been reduces to one fourth of the initial number but we can handle multilevel signals. The new representation allows to obtain phase diagram with a higher information content. A closed orbit will represent periodic signals, with a pattern depending on the signal characteristics. An example is given in Fig. 2, where a periodic signal appears. It is possible to see that after a certain pattern, the trajectory get back to same initial point.

These periodic trajectories are obtained for almost any relation between the external and internal times of the OPLC. But this situation is drastically changed when the relation gets a value close to infinity. That means that the internal time gets a value close to zero. Under this condition, the output of the system becomes chaotic and the corresponding phase diagram covers

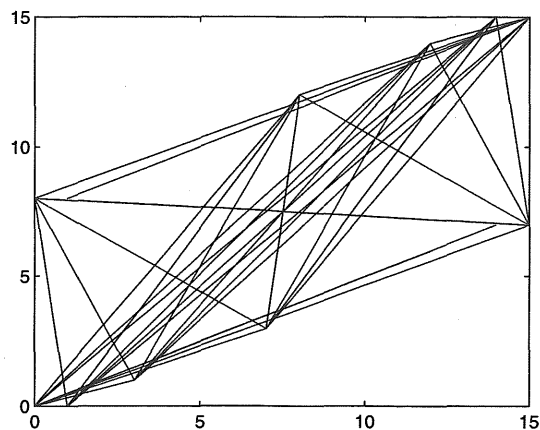


Fig. 3.- Phase Diagram of a periodic signal

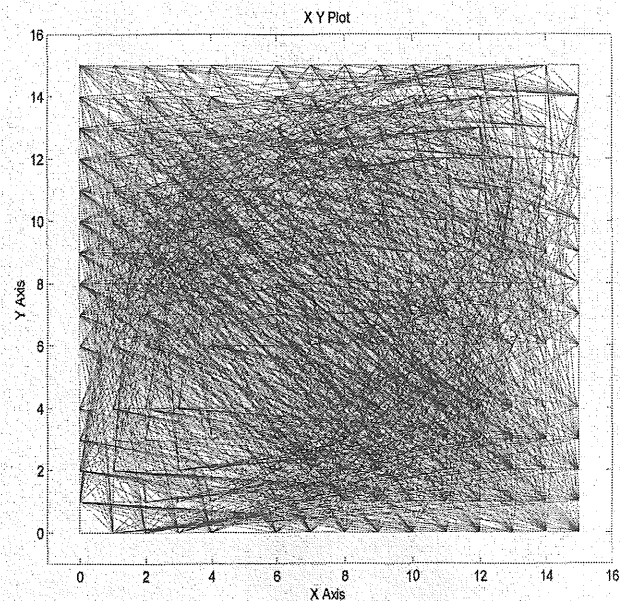


Figure 4.- Phase Diagram of Digital Chaos Signal.

almost the whole surface of the diagram and it is not possible to get back to the initial point after a certain number of orbits. An example is given in Fig. 3.

The analysis of these signals are, again, much more difficult than the corresponding to an analogue signal. The possibilities to extract numerical information about its properties are almost impossible with conventional techniques. Methods as those derived from Lyapunov Exponent are very difficult to be employed. We have reported a possible way to study the characteristics of the obtained signal with the help of the Lempel and Ziv method. The results have been reported in ⁴ and give a possible way to know the characteristics of the obtained signal with some set of boundary conditions. It give a certain number, named "complexity" of the signal, that when it is close to the unity indicates that the signal is almost chaotic. This information constitutes a valuable tool to determine the conditions of the signal.

But if one needs information related with the evolution of the signal depending on the value adopted by the ratio between external and internal times, above indicated methods are no useful. It is important to know the characteristics of the signal. But it is very important, too, to know the route this signal has adopted to reach that particular state and what should be the evolution if the critical parameter changes again its value. This is the route to chaos in conventional systems.

3. ANALYSIS OF THE EVOLUTION TO CHAOS

The method we have adopted to study the evolution of the signal generated by the Optically Programmable Logic Gate has been the representation of the number of points achieved by the signal for each value of the control parameter. In our case, as it has been pointed out before, this critical parameter is the ration between the external and the internal time of the OPLC. We have kept constant the external time and we have varied the internal from large values to values close to zero.

In a conventional route to chaos, as the one obtained, for example, by the logistic equation, the parameter to be represented in ordinates is the frequency or frequencies obtained for a certain value of the critical parameter. In this way, for this value, the system behaviour is a periodic signal with certain frequency content. The situation when the signal is composed by a train of binary digits is much more difficult to analyze. Every bit has the same time length and, between bits, there is always the same time length.

It is because that we have adopted a new method. It gives similar information than in the analog case and, at the same time, its approach is more intuitive. The first step is to group bits in sets of eight instead the previous groups of four bits employed in other papers. In this way we have 256 levels for each representation point. We have increased from 8 in

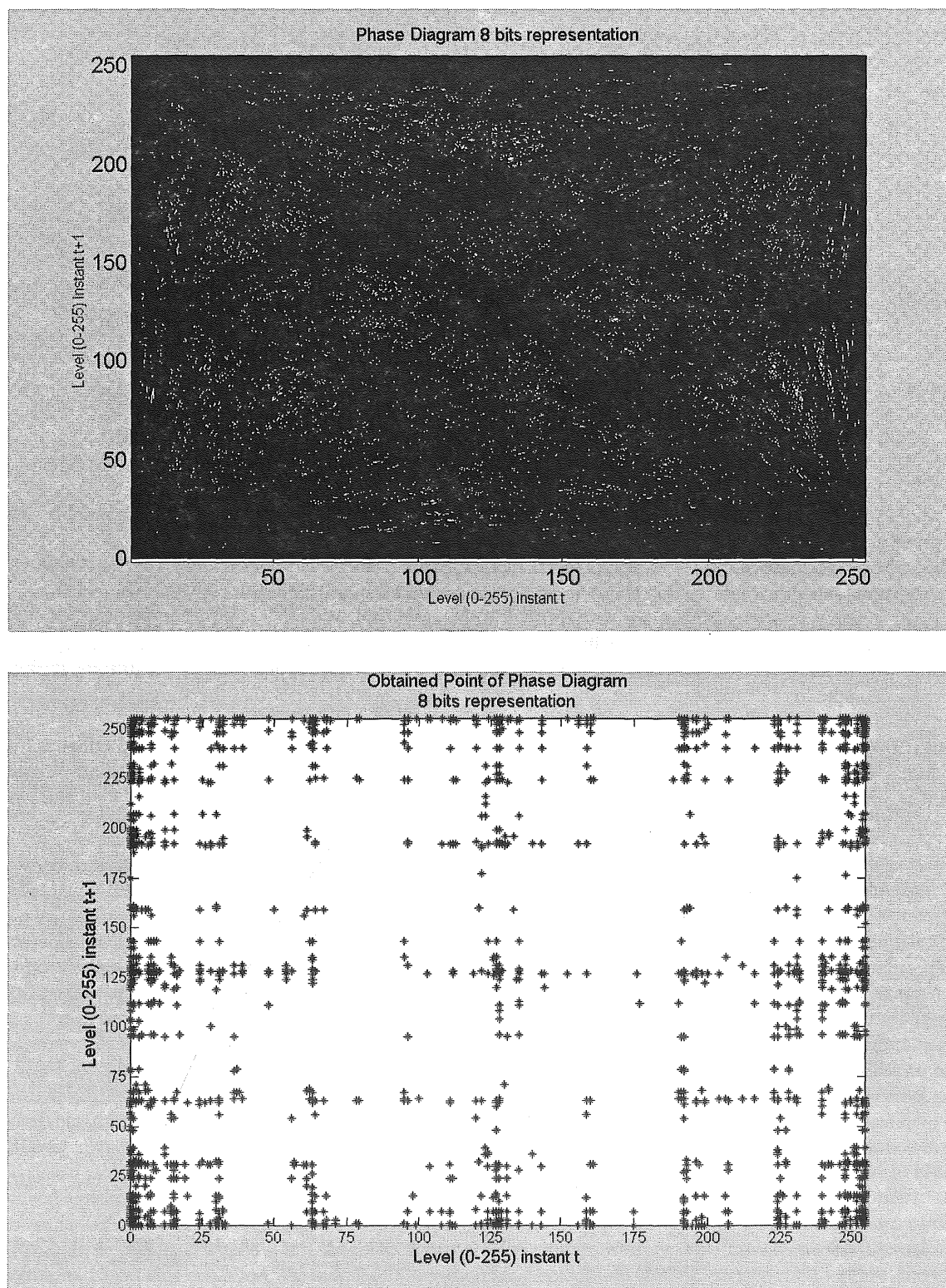


Fig. 5.- Phase diagram of a chaotic signal with 256 reference levels (a) trajectories (b) obtained points

previous papers to these 256. With this new approach Fig. 4 changes now to the representation given in Fig. 5 where there are 256 numbers in each one of the coordinate axis. As we can see there is no new information by this increasing in the number of levels. Hence this new approach must be changed to another one if more information is needed.

The approach we have adopted is to draw a diagram equivalent to the route to chaos employed in analog signals. We have studied the number a certain point is crossed by the chaos trajectory. This data was impossible to obtain in Figs. 4 – 5. The new representation may give two different types of information. The first one is, as we have pointed out, the number of times a certain point is crossed by the trajectory, after considering a long time interval. The second one is to represent the points that have been crossed for every internal delay time taken.

The first analysis we have performed is represented in Fig. 6. We have taken a total of 300000 simulation points. The external delay time is 200. We have maintained this time in every one of our simulations. The internal delay time has been changed from 21 to 0 in steps of 1 unit. As it may be seen, the number of crossed points is very low from 21 to 1. The number is 6 for every delay time. Just for a time of 12, this number reduces to 3. The obtained results give two important conclusions. The first one is that the possibility to obtain chaos is larger when the internal delay time approaches to zero. The second one is that the internal detail of the figure is very low. This is consequence of the large variation adopted for variations in time. In order to get better information, smaller steps in time should be adopted.

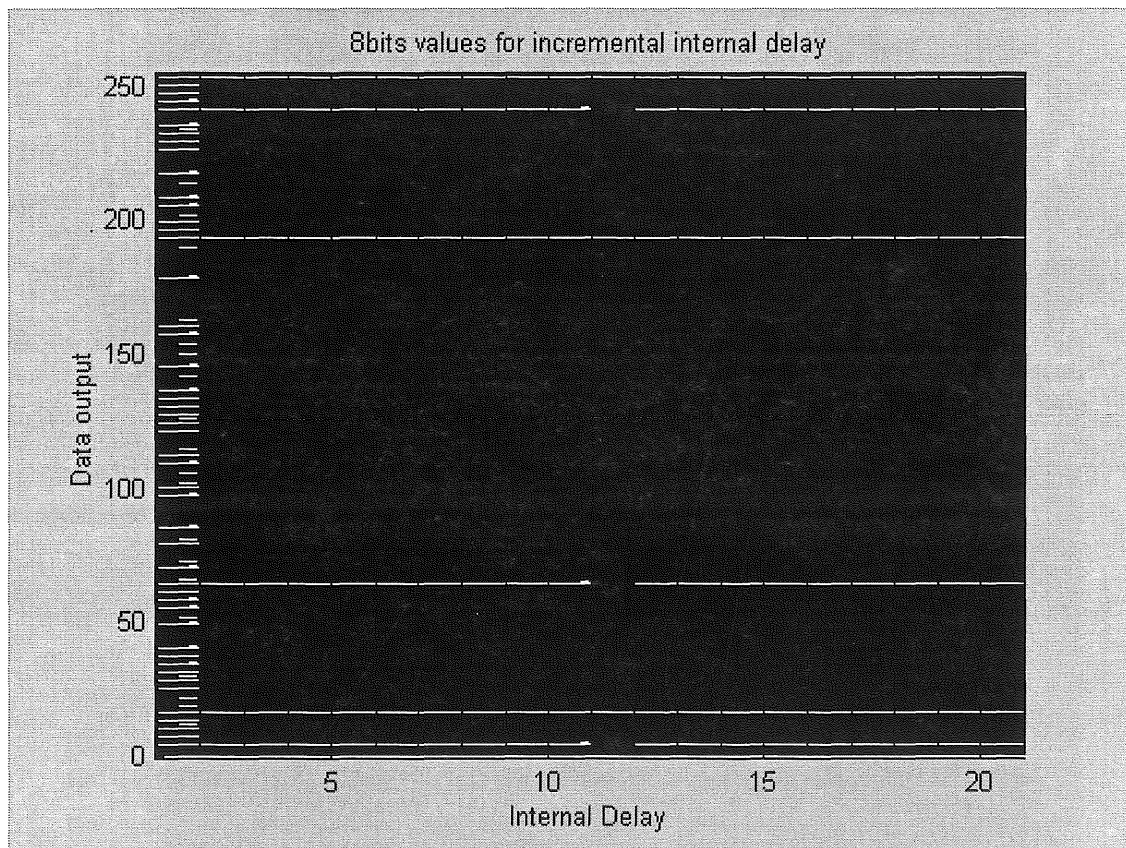


Fig. 6.- Diagram of the route to chaos for external delay time of 200 units changes in internal delay times from 21 to 0, in steps of 1 unit. Ordinate gives the obtained point in a representation of 256 levels.

Fig. 7. gives the variation in obtained points when the increasing steps for internal delay time reduce to 0.1. The represented interval covers now from 5.5 to 0 and the number of points is now 400000. As it can be seen, the internal details in the figure have now increased significantly. There are new regions covered now by points that were previously empty. This indicates the importance of the precision level adopted in the simulation. Some more information may be obtained if

we adopt a logarithm representation. This representation appears in Fig. 8. The same increase in number of points when we approach to zero, than in previous cases, is present now with this approach too.

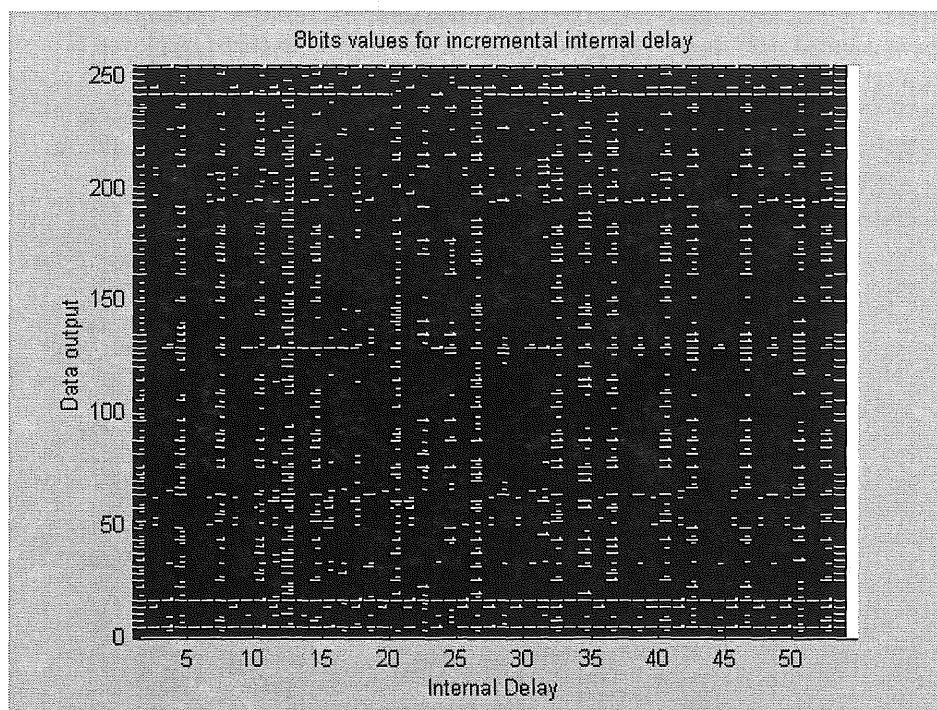


Fig. 7.- Diagram of the route to chaos for external delay time of 200 units changes in internal delay times from 5.5 to 0, in steps of 0.1 units. Ordinate gives the obtained point in a representation of 256 levels.

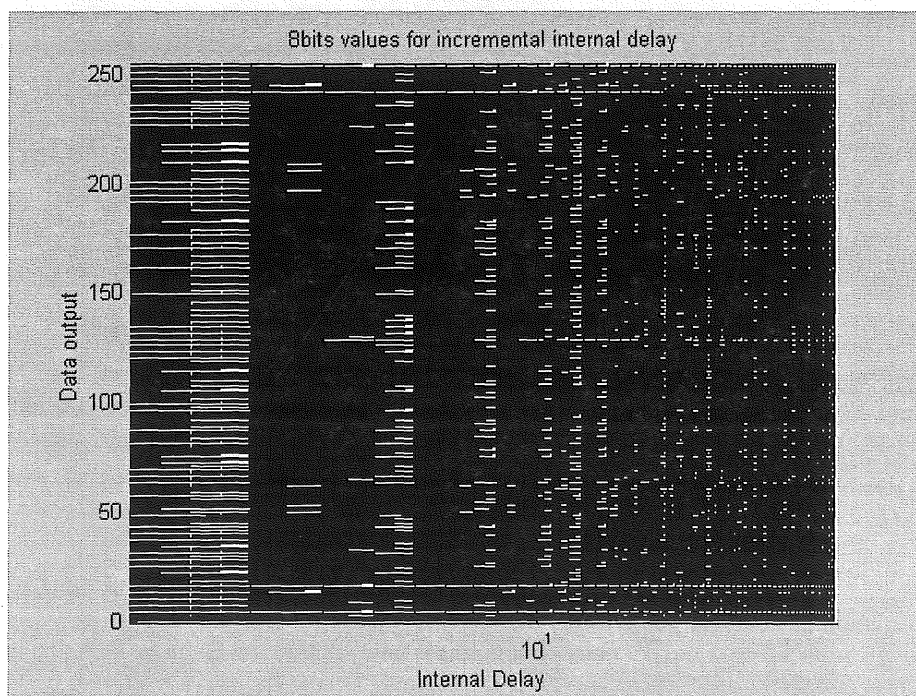


Fig. 8.- Diagram of the route to chaos for external delay time of 200 units changes in internal delay times from 5.5 to 0, in steps of 0.1 units. Ordinate gives the obtained point in a representation of 256 levels. Abscises axis is in logarithmic units.

The above representations does not give information about the number of times a certain point is crossed in these diagrams. In order to get an idea about this fact, we have represented in Fig. 9 some information about the results obtained for internal delays times of 8, 7, 6, 2 and 1. These results are shown just an example of new information that may be obtained and applied to a further analysis of digital chaotic signals.

Finally, and as a final indication of the behaviour of the system when internal delay time moves, Fig. 10-11 gives the tendency of the number of points crossed for each value of time. The represented values run from 10 to 0 time units in steps of 1 time unit (Fig. 10) and 0.1 time units (Fig. 11). There is clear approach to larger numbers when internal delay time get smaller being the limit value 256, as it is clear from the adopted representation.

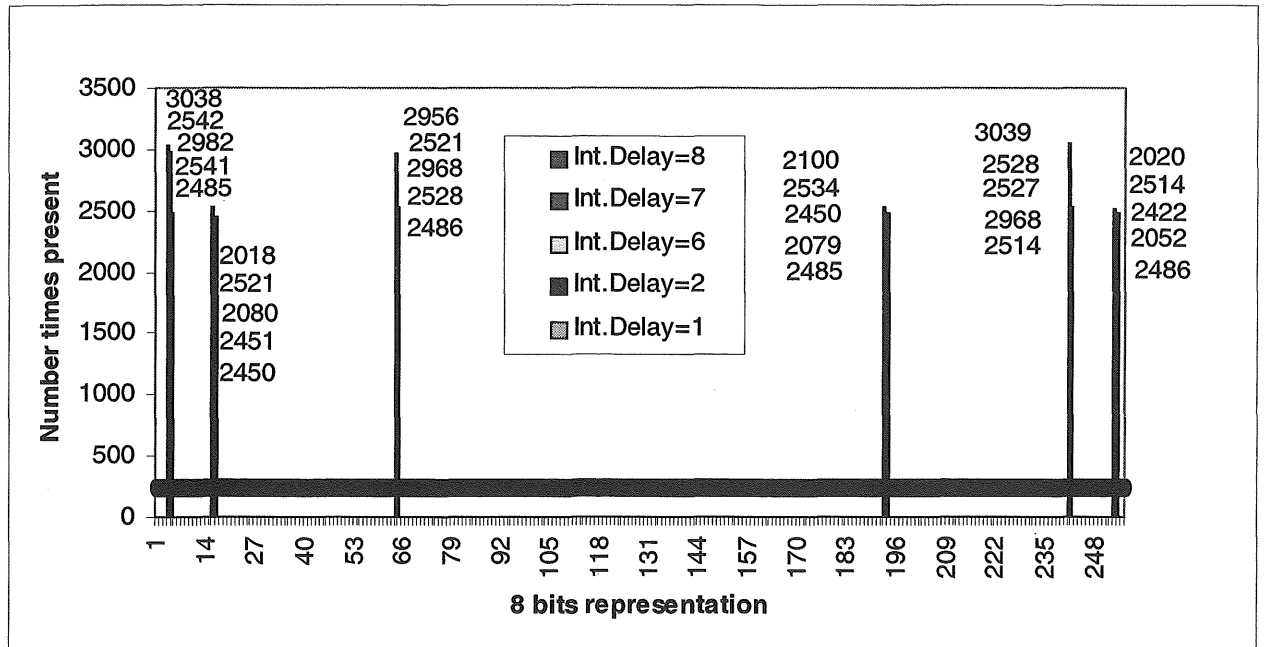


Fig. 9.- Number of times that particular points are crossed at certain internal delay times.

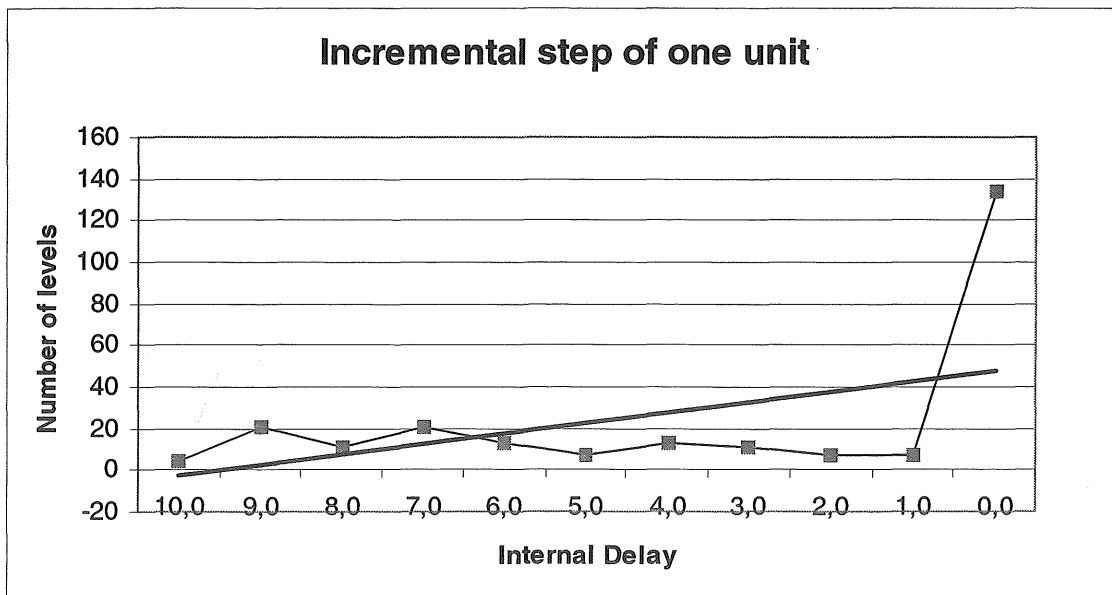


Fig. 10.- Tendency of number of obtained points as a function of internal delay time in steps of 1. time units.

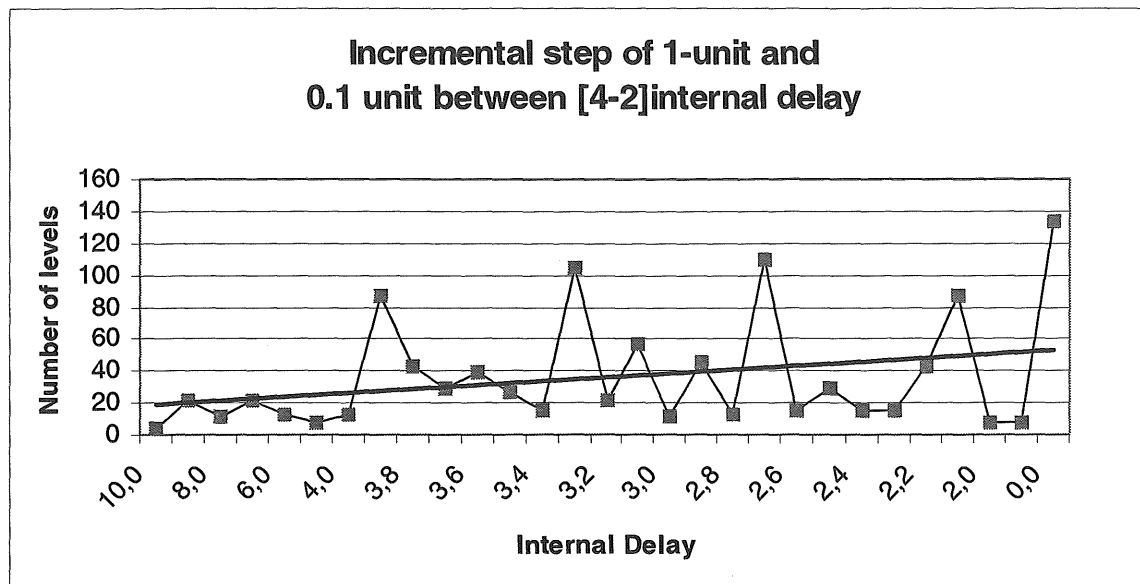


Fig. 11.- Tendency of number of obtained points as a function of internal delay time in steps of 0.1. time units.

4. CONCLUSIONS

We have reported some possible ways to analyze chaotic digital signals. Our study has centred on the influence of the internal delay time of an optically programmable logic cell where the chaos is obtained for certain values of cell parameters. We have shown that is possible to see the evolution to chaos as a function of the delay time as well as the number of time a certain value is crossed in the trajectory. These representations have a close parallelism with similar representations had in analogue signals. We think that the tools reported in this paper, as well as some others reported in other places¹⁰⁻¹¹, may serve to study more carefully chaotic digital signals, nor previously studied before.

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